RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FOURTH SEMESTER EXAMINATION, MAY 2025

SECOND YEAR (BATCH 2023-27)

Date : 13/05/2025 **COMPUTER SCIENCE**

Time : 11.00 am – 1.00 pm **Paper : 4CMSMIC1** Full Marks : 50

Answer **any five** questions**:** [5×10]

1. a) Convert $(10110.110)_2$ to $(?)_{10}$ and $(8A7C)_{16}$ to $(?)_8$
   b) State the properties of NAND and NOR gates and explain why they are called universal gates.
   c) Design a 4-bit binary subtractor circuit using one 4-bit adder IC and other gates, and explain the working principle using 2's complement method. [2+2+6]

2. a) Design a 4-to-16 decoder using two 3-to-8 decoders and explain the working principle with a logic diagram.
   b) Simplify the function $f(A,B,C)=\Sigma m(0,1,2,4,6,7)$ using k-map. And implement this functions using basic gates. [4+(3+3)]

3. a) Implement the functions $f(A,B,C,D)=\Sigma m(0,1,2,5,7)$ using one 4×1 multiplexer.
   b) What is the function of a decoder in digital circuits? Give one practical application.
   c) Explain the working of a BCD adder using an example and truth table. [4+2+4]

4. a) Design a full adder using two half adders and an OR gate. Explain the working principle with a truth table and circuit diagram.
   b) Design a full subtractor using basic gates with the help of truth table of full subtractor. [6+4]

5. a) Design an S-R latch using only two NOR gates. Compare its forbidden state with that of S-R latch designed with only two NAND gates.
   b) What is race-around condition and for which type of latches it is unavoidable? What method can be used to encounter race-around?
   c) Compare JK flip-flop with Master-Slave JK flip-flop. Convert Master-Slave JK flip-flop to obtain D and T-type flip-flops. Also mention applications of D and T flipflops. [(1+2)+(2+1)+(1+2+1)]

6. a) Why are Counters designed with flip-flops operated in toggle mode.
   b) Ring counter and Johnson counter are basically sequence generator but not counters – explain briefly.
   c) Design and state the working of a 4bit parallel in serial out (PISO) register. [2+3+5]

7. a) Differentiate between asynchronous and synchronous counters.
   b) State the sub-classes of asynchronous counters. On what basis this classification is done?
   c) Draw the circuit diagram of a 4-bit synchronous UP-counter designed with T-type flip-flops. Also mention the design logic and working of the circuit. [2+(1+2)+(1+2+2)]

8. a) Simplify $(A+B)(B+C)(A+B'+C)$ and $(AB+BC+AB'C)$. Here B' represents complement of B.
   b) A digital logic circuit is such that, it can take 4-bit binary input data and produces an output high state whenever the decimal equivalent of the input is divisible by decimal three. Obtain the truth table and also design the required circuit using basic gates.
   c) Find out minimum SOP and POS expressions for the function given below: $F(W,X,Y,Z)=\Sigma m(0,1,4,6,8,14,15).\ \Sigma(2,3,9)$.
   d) In canonical representation of a switching function if m_i and M_i represent the i'th minterm and maxterm respectively then show that $m_i.M_i = 0$ and $m_i + M_i = 1$. [(1.5+1.5)+3+3+1]

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